



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,479	09/13/2001	Siegfried Schweidler	PD990014	6074
	7590	04/23/2010	EXAMINER	
Joseph S Tripoli Thomson Multimedia Licensing PO Box 5312 Princeton, NJ 08540			LI, ZHUO H	
			ART UNIT	PAPER NUMBER
			2185	
			MAIL DATE	DELIVERY MODE
			04/23/2010	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



UNITED STATES PATENT AND TRADEMARK OFFICE

---

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/936,479  
Filing Date: September 13, 2001  
Appellant(s): SCHWEIDLER ET AL.

\_\_\_\_\_  
Paul Kiel (Reg. No. 40,677)  
For Appellant

**EXAMINER'S ANSWER**

Art Unit: 2185

This is in response to the appeal brief filed February 2, 2010 appealing from the Office action mailed August 06, 2009

**(1) Real Party in Interest**

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The following is a list of claims that are rejected and pending in the application:

- A. Claims 1-9 are pending.
- B. Claims 1-9 are stand rejected and under appeal.

**(4) Status of Amendments After Final**

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

**(5) Summary of Claimed Subject Matter**

Art Unit: 2185

The examiner has no comment on the summary of claimed subject matter contained in the brief.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

**(7) Claims Appendix**

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

**(8) Evidence Relied Upon**

6,961,890	Smith	11-2005
6,324,178	Lo et al.	11-2001
5,404,166	Gillard et al.	04-1995
5,410,546	Boyer et al.	04-1995

**(9) Grounds of Rejection**

Art Unit: 2185

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 4, 5, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US PAT. 6,324,178 hereinafter Lo) in view of Smith (US 6,961,890) and Gillard et al. (US PAT. 5,404,166).

Regarding claim 1, Lo discloses a method for the management of data received via a serial data bus (240 or 250, figure 2A) in a receiving device (220, figure 2A and col. 4 line 47 through col. 5 line 14) comprising the steps of receiving data transmitted in bus packets having a variable length (col. 5 lines 24-35, data packets of a first communication domain are different

Art Unit: 2185

from data packets of a second communication domain such that data packets received in the receiving device are obviously in variable length), each bus packet having a header (326, figure 3A) and a payload data field (324, figure 3A), the payload data field being divided into a plurality of data blocks having a defined length (data blocks and each data block has 32 bits, figure 8A), a combination of a defined number  $n$  of data blocks forming a data source packet of fixed length (col. 8 line 6 through col. 9 line 9, i.e., assembly a new data packet by a combination of a defined number  $n$  of block), section-by-section transmission of the data source packet within the framework of data blocks being permitted (col. 9 lines 10-40, i.e., accessing data payload field and broadcasting data until termination). Lo differs from the claimed invention in not specifically teaching a data block consisting of a plurality of data words and the plurality of data words being a fixed amount. However, it is old and notoriously well known in the art of having a data block consisting of a plurality of data words and the plurality of data words being a fixed amount, for example see Smith (figures 1-2 and col. 3 line 49 through col. 5 line 17, i.e., a data block, 100 or 200, consisting a plurality of data words, 202 or 204, the plurality of data words being a fixed amount, such as 16 bit code or 24 bit code) in order to provide the data integrity required in response to changing condition. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Lo in having the data block consisting of a plurality of data words and the plurality of data words being a fixed amount, as per teaching of Smith, in order to provide the data integrity required in response to changing condition. The combination of Lo and Smith differs from the claimed invention in not specifically teaching the step of carrying out a modulo- $n$  counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source

Art Unit: 2185

packet is signaled to a memory management device at the beginning of the next counting interval. However, Gillard teaches subsequent storage of data or error correction encoding generally operating on fixed length data word (col. 1, lines 23-25) such that one skill in the art would recognize each data block within the payload data field as shown on Lo consisting of a plurality of data words being a fixed amount as taught by Gillard. In addition, Gillard teaches carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval, i.e., format accumulator (120) generates a 5-bit output signal representing a modulo-32 count of the code length received during the formatting of a current data block, count accumulator (125) maintains a count of the cumulative lengths of payload data field related to the video data stream, these counts are then summed to generate a total count, when the total count reaches the available length of the video data section, and end of block signal is generated by the count accumulator, a boundary accumulator (126, figure 3) incorporate with pointer, count accumulator and header with starting address indicative of the position of the video data, to determining the end of each variable length video data stream in a fixed length blocks (col. 4 line 34 through col. 5 line 35), thereby providing data format conversion in a way that keep pace with the overall data rate. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Lo and Smith in carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the

Art Unit: 2185

next counting interval, as per teaching of Gillard, in order to provide data format conversion in a way that keep pace with the overall data rate.

Regarding claim 4, the combination of Lo, Smith and Gillard differs from the claimed invention in not specifically teaches wherein the defined number  $n$  of data blocks of a data source packet corresponds to the number 8 and the modulo- $n$  counting is correspondingly modulo-8 counting. However, it is old and notoriously well known in the art of having the defined number of  $n$  data blocks corresponding to the number of 2 to power  $x$ , where  $x = 1, 2, 3, \dots$ , in which 8 is equal to 2 to power 3. In addition, utilizing modulo-8 counter do not have a disclosed purpose nor overcome any deficiencies in the prior art such that the number of  $n$  of data blocks of a data source packet may contain any number, i.e., 2, 4, 8, .... Noted Gillard teaches the variable video data frame stored in a plurality of fixed length data block in 8-bit data words (col. 5 line 55 through col. 6 line 1), and count accumulator (125) maintains a count of the cumulative lengths of payload data field related to the video data steam, these counts are then summed to generate a total count, when the total count reaches the available length of the video data section, and end of block signal is generated by the count accumulator, a boundary accumulator (126, figure 3) incorporate with pointer, count accumulator and header with starting address indicative of the position of the video data, to determining the end of each variable length video data steam in a fixed length blocks (col. 4 line 34 through col. 5 line 35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Lo and Gillard in utilizing modulo-8 counter for counting 8 of data blocks of a data source packet, as disclosed supra, because applicant does



Art Unit: 2185

not disclose that the number 8 and modulo-8 counting, as opposed to other size, overcome a deficiency in the prior art or for any stated purpose.

Regarding claim 5, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 8, Gillard discloses the counter, i.e., count accumulator (125) by which data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as defined as belonging a data block (col. 4 line 34 through col. 5 line 35).

Regarding claim 9, Lo teaches IEEE 1394 serial bus communication standard becoming a popular standard adopted by manufacturers of computer systems and peripheral components for its high speed and interconnection flexibilities (col. 1 lines 31-35).

3. Claims 2-3 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US PAT. 6,324,178 hereinafter Lo) in view of Smith (US 6,961,890) and Gillard et al. (US PAT. 5,404,166) as applied in claims above, and further in view of Boyer et al. (US PAT. 5,410,546 hereinafter Boyer).

Regarding claims 2-3, the combination of Lo and Gillard differs from the claimed invention in not specifically teaches each bus packet being subject to CRC checking and the checking results being buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has been transmitted without transmission errors, wherein a reference count reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data block is effected

Art Unit: 2185

and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence. However, Boyer discloses a data transferring device (figure 1) comprising a blocking/compression unit (105) compresses the data and transmits the data over bus (108) in packets to both Page CRC generator (101) for CRC generation and to page buffer memory (102) for temporary storage, and CRC checker (104) computes a CRC code for the entire page buffer as each byte is transmitted over bus (110) to block storage device (107), and may invoke appropriate error recovery procedures when it detects a compare error from CRC checker (col. 7 line 11 through col. 8 line 63). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Lo and Gillard in having each bus packet being subject to CRC checking and the checking results being buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has been transmitted without transmission errors, wherein a reference count reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data block is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence, as per teaching by the data transfer device of Boyer, because it assures the integrity of the data at all times between receipt from the compression unit and transmission to the storage device, and permits these CRC computations and combinations to proceed as the data is received without loss of performance at the high data rates common in current high density tape storage subsystem (col. 5 lines 28-34).

Art Unit: 2185

Regarding claims 6-7, the limitations of the claims are rejected as the same reasons set forth in claims 2-3.

### **(10) Response to Argument**

Appellant's arguments filed 2/2/2010 have been fully considered but they are not persuasive.

#### **A. Claim 1, 4, 5, 8 and 9 are not properly rejected under 35 U.S.C. §103(a) over Lo in view of Smith and Gillard.**

##### 1. Claim 1

In response to appellant's arguments that the combination of Lo, Smith and Gillard fails to teach or suggest "the payload data field being divided into a plurality of data blocks having a defined length, a data block consisting of a plurality of data words, the plurality of data words being a fixed amount, as recited in claim 1, examiner respectfully disagrees because Lo clearly illustrate fields within exemplary generic and asynchronous IEEE1394 data packets as shown in figures 3A, which includes packet header field (326) and data payload field (324). The payload field is divided into a plurality of data block quadlets, i.e., read as data blocks, having a defined length (see data block quadlets 1 and 2 in figures 8A and 8B that each data block quadlet contains 32 bits), in addition, the "one single data block" in figures 8A and 8B as pointed out by appellant, examiner respectfully disagree because the labeled "data block" in figures 8A and 8B is just an exemplary frame formats used by the IEEE1394 domain that including header section (352) and data block section, i.e., payload section as defined in Figure 3A, that including a plurality of data block quadlets, i.e., a plurality of data blocks that has defined length with 32 bits

Art Unit: 2185

in each of the data block quadlets (col. 9 line 41 through col. 10 line 65). Lo differs from the claimed invention in not specifically teaching that a data block quadlet consist a plurality of data words, the plurality of data words being a fixed amount. However, Smith teaches a data structure (200, figure 2) include a data pool (202, figure 2 read as data block), which the data pool includes a plurality of data words (212, figure 2), the plurality of data words being a fixed amount (col. 4 lines 32-37). Thus, the combination of Lo and Smith teaches the limitations of “the payload data field being divided into a plurality of data blocks having a defined length, a data block consisting of a plurality of data words, the plurality of data words being a fixed amount, as recited in claim 1. In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to appellant's argument that there is no reason for a skilled person to combine Lo and Smith because their teachings are cumulative, as both teach a single data block with a plurality of data words, examiner respectfully disagrees because Smith clearly teaches the allocation of the data structure maximizing data integrity (col. 2 lines 15-19) such that one skill in the art would modify data block quadlets of Lo in having the structure as taught by Smith in order to maximize data integrity. Therefore, examiner has established a rationale for combining Lo and Smith in accordance with the Office action.

In view of at least the foregoing, examiner submits that claim 1 is rejected under the combination of Lo, Smith and Gillard, and the rejection should be affirmed.

Art Unit: 2185

## 2. Claim 5

Similarly, Appellant's independent claim 5, in part, requires: "the payload data field being divided into a plurality of data blocks having a defined length, a data block consisting of a plurality of data words, the plurality of data words being a fixed amount." Claim 5 is different from claim 1, however the relative response of appellant's argument used above for claim 1 may be applied to claim 5. Therefore, examiner repeats the above response of arguments for claim 1 and applies them to claim 5. Thus for at least the reasons discussed above for claim 1, claim 5 is rejected under the combination of Lo, Smith and Gillard and the rejection should be affirmed.

## 3. Claims 4, 8 and 9

Claims 4, 8 and 9 respectively depend from one of claims 1 and 5, and inherit all the respective features of their respective base claim. Therefore, claims 4, 8 and 9 are rejected for at least the reason that they respectively depend from claims 1 or 5, with each claim containing further distinguishing features, and the rejection should be affirmed.

## **B. Claims 2, 3, 6 and 7 are not properly rejected under 35 U.S.C. §103(a) over Lo in view of Smith and Gillard, and further in view of Boyer.**

Claims 2, 3, 6 and 7 respectively depend from one of claims 1 and 5, and inherit all the respective features of their respective base claim. Therefore, claims 2, 3, 6 and 7 are rejected for at least the reason that they respectively depend from claims 1 or 5, and the rejection should be affirmed.

Art Unit: 2185

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Zhuo H Li/

Examiner, Art Unit 2185

Conferees:

/Kevin L Ellis/  
Supervisory Patent Examiner, Art Unit 2117

/Sanjiv Shah/  
Supervisory Patent Examiner, Art Unit 2185